Abstract of the Disclosure

A source terminal layer, a gate terminal layer, and a drain terminal layer are disposed on main surfaces, opposite to each other, on main surfaces of a semiconductor substrate. These terminal layers are laid out on the respective main surfaces with such sizes as to fall within the areas of the respective main surfaces and joined to their corresponding source, gate, and drain electrodes. A power MOSFET is packaged on a circuit board such that the respective main surfaces intersect substantially at right angles to the circuit board. By a terminal board isolating step or a method of evaporating a metal layer onto the source, gate, and drain electrodes, the power MOSFET is formed with the source terminal layer, gate terminal layer, and drain terminal layer at the stage of a semiconductor wafer.